In the Claims:

Please amend claims 1-9 as follows:

1. (currently amended) A method for implementing enhanced performance and reduced leakage current for application specific integrated circuit (ASIC) designs comprising the steps of:

identifying standard voltage threshold (SVT) circuits in a circuit library;

for each SVT circuit, replacing each SVT P-channel field effect transistor (PFET) with a low voltage threshold (LVT) PFET and maintaining each N-channel field effect transistor (NFET) having a standard voltage threshold (SVT) to provide a hybrid alternate voltage threshold (AVT) circuit; and

saving each said AVT circuit in an alternate circuit library.

2. (currently amended) A method for implementing enhanced performance and reduced leakage current as recited in claim 1 wherein the step of replacing each SVT PFET with a low voltage threshold (LVT) PFET includes the step of adding a low voltage threshold (LVT) mask over each said SVT PFET.

3. (currently amended) A method for implementing enhanced performance and reduced leakage current as recited in claim 2 wherein the step of adding a low voltage threshold (LVT) mask over each said SVT PFET includes the step of adding a single shape defining said low voltage threshold mask over an Nwell region to convert each said SVT PFET ~~PFETs~~ to said LTV PFET.

4. (currently amended) An alternate voltage threshold (AVT) circuit library comprising:

a plurality of hybrid AVT circuits, each said hybrid AVT circuit including

a plurality of P-channel field effect transistors (PFETs) and a plurality of N-channel field effect transistors (NFETs);

each P-channel field effect transistor (PFET) having a low voltage threshold (LVT); and

each N-channel field effect transistor (NFET) having a standard voltage threshold (SVT).

5. (currently amended) An alternate voltage threshold (AVT) circuit library as recited in claim 4 wherein said hybrid AVT circuits include a corresponding standard voltage threshold (SVT) circuit having a low voltage threshold (LVT) mask added over each said SVT PFET to convert each said SVT PFET to said LVT PFET.

6. (currently amended) An alternate voltage threshold (AVT) circuit library as recited in claim 4 wherein each said LVT PFET ~~are~~ is provided in an Nwell Region isolated from each said NFET in each said hybrid AVT circuit.

7. (currently amended) A computer program product for implementing enhanced performance and reduced leakage current for application specific integrated circuit (ASIC) designs in a computer system, said computer program product including instructions executed by the computer system to cause the computer system to perform the steps of:

identifying standard voltage threshold (SVT) circuits in a circuit library;

for each SVT circuit, replacing each SVT P-channel field effect transistor (PFET) with a low voltage threshold (LVT) PFET and maintaining each N-channel field effect transistor (NFET) having a standard voltage threshold (SVT) to provide a hybrid alternate voltage threshold (AVT) circuit; and

saving each said AVT circuit in an alternate circuit library.

8. (currently amended) A computer program product as recited in claim 7 wherein the step of replacing each SVT PFET with a low voltage threshold (LVT) PFET includes the step of adding a low voltage threshold (LVT) mask over each said SVT PFET.

9. (currently amended) A computer program product as recited in claim 8 wherein the step of adding a low voltage threshold (LVT) mask over each said SVT PFET includes the step of adding a single shape defining said low voltage threshold mask over an Nwell region to convert each said SVT PFET to said LTV PFET.